Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended). A circuit device (1), comprising at least a first connection (3a) and a second connection (3b), whereby a single clock pulse (CLK, CLK_T) can be applied to the first connection (3a) or a differential clock pulse (CLK, CLK_T, /CLK, $/CLK_T$) can be applied to the first and second connections (3a, 3b), and a detection facility (2) to detect whether there is a differential clock pulse (CLK, CLK_T, /CLK, $/CLK_T$) present at the first and second connections (3a, 3b) or a single clock pulse (CLK, CLK_T) present at the first connection (3a), the detection facility (2) having a first state, if a differential clock pulse (CLK, CLK_T, /CLK, $/CLK_T$) is present at the first and second connections (3a, 3b), in which a first output signal is provided, and a second state, if a single clock pulse (CLK, CLK_T) is present at the first connection (3a), in which a second output signal different than the first output signal is provided.

Claims 2 and 3 (canceled).

4 (currently amended). A circuit device (1) according to ~~claim 3~~ Claim 8, in which the comparison device (24) comprises a differential amplifier.

5 (currently amended). A circuit device (1) according to Claim [[3]] 8, in which the comparison device (24) emits a pulse, more specifically a clock pulse detection signal, when the level of the signal present at the connection (3b) exceeds or falls below a predetermined level (VREF), in particular, the level of the reference signal (VREF).

6 (currently amended). A circuit device (1) according to Claim [[3]] 8, in which the comparison device (24) emits a signal, more specifically a clock pulse detection signal, when the level of the signal present at the connection (3b) first exceeds a predetermined, first level (VREF + ΔU_1), and then falls below a predetermined second level (VREF - ΔU_2) that differs from the first level.

7 (currently amended). A circuit device (1) according to Claim [[3]] 8, in which the comparison device (24) then emits a pulse, more specifically a clock pulse detection signal, when the level of the signal present at the connection (3b) first falls below a predetermined first level and then exceeds a predetermined second level that differs from the first level.

8 (currently amended). A circuit device (1) ~~according to Claim 3, which also comprises~~ comprising:

at least a first connection (3a), to which a clock pulse (CLK, CLK_T) can be applied, and a second connection (3b), to which a clock pulse (/CLK, /CLK_T) can be applied;

a detection facility (2) which in determining whether a clock pulse (/CLK, /CLK_T) is present at the second connection (3b), determines whether there are differential clock pulses (CLK, CLK_T; /CLK, /CLK_T) present at the connections (3a, 3b), or whether there is a single clock pulse (CLK, CLK_T) present at the first connection (3a), but not at the second connection (3b);

a comparison device (24) for comparing the signal present at the connection (3b), in particular the clock pulse (/CLK, /CLK_T) applied thereto, with a reference signal (VREF); and

a counter device (7), in particular for detecting the number of pulses, particularly clock pulse detection signals, emitted by the comparison device (24).

9 (previously presented). A circuit device (1) according to Claim 8, in which, when the number (Z) of pulse, in particular clock pulse detection signals emitted by the comparison device (24), and detected by the counter device (7), is larger then or equal to a predetermined number (Z_0), it is determined that the clock pulse (/CLK, /CLK_T) is present at the connection (3b).

10 (currently amended). A semi-conductor component that comprises at least one circuit device (1) comprising:

at least a first connection (3a), to which a clock pulse (CLK, CLK_T) can be applied, and a second connection (3b), to which a clock pulse (/CLK, /CLK_T) can be applied; and

a detection facility (2) which in determining whether a clock pulse (/CLK, /CLK_T) is present at the second connection (3b), determines whether there are differential clock pulses (CLK, CLK_T; /CLK, /CLK_T) present at the connections (3a, 3b), or whether there is a single clock pulse (CLK, CLK_T) present at the first connection (3a), but not at the second connection (3b),

the detection facility (2) having a first state, if differential clock pulses (CLK, CLK_T; /CLK, /CLK_T) are present at the connections (3a, 3b), in which a first output signal is provided, and a second state, if a single clock pulse (CLK, CLK_T) is present at the first connection (3a), in which a second output signal different than the first output signal is provided.

11 (original). A semi-conductor component according to Claim 10, which is a DDR (double data rate) component, in particular a DDR memory component.

12 (original). A semi-conductor component according to Claim 10, in which the memory component is a DRAM (dynamic random access memory).